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SCR Devices with Deep-N-Well structure for On-Chip ESD protection  
circuits

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BACKGROUND OF THE INVENTION

**Field of the Invention**

The present invention relates in general to a silicon-controlled rectifier, SCR, component with a deep N-well structure. In particular, the present invention relates to an SCR component of an electrostatic discharge (ESD) protection circuit.

**Description of the Related Art**

Electrostatic discharge (ESD) represents one of the main threats to reliability in semiconductor products, especially in scaled-down CMOS technologies. Due to low breakdown voltage of thinner gate oxide in deep-submicron CMOS technologies, an efficient ESD protection circuit must be designed and placed on every input pad to clamp the overstress voltage across the gate oxide of the internal circuit.

Due to the low holding voltage ( $V_{hold}$ , about 1V in CMOS process) of the SCR, power ( $Power = I_{ESD} \times V_{hold}$ ) generated by the SCR device during the ESD stress is less than other ESD protection devices (such as diode, MOS, BJT, or field-oxide device) in CMOS technologies. Therefore, the SCR device can sustain a much higher ESD level within a smaller layout area in the CMOS IC's. Thus, SCR devices have been used as the main ESD-clamped devices in

several ESD protection circuits. In traditional CMOS technologies, well regions and heavy-doped diffusions are laterally deposited on a substrate to form an SCR device also known as lateral SCR (LSCR). The traditional input ESD protection circuit with the LSCR device is shown in Fig.1a, and the device structure of the SCR device in CMOS process is shown in Fig.1b. The PNPN structure of the LSCR is formed by the p+ diffusion 10, the N-type well 12, the P-type substrate 14 and the N+ diffusion 16. The typical I-V curve on the SCR device in CMOS process is shown in Fig.1c. The LSCR devices in Fig.1b have a trigger voltage  $V_{trigger}$  approximately equal to the breakdown voltage of the P-N junction between the N-well 12 and the p-substrate 14, about 30~40V, which is generally greater than the gate-oxide breakdown voltage (15~20 volt) of CMOS devices. Therefore, SCR devices need a secondary protection ESD circuit (as the resistor and MESD shown in Fig.1a) to ensure overall ESD protection.

In order to effectively protect output buffers by using SCR devices, an LVTSCR (low-voltage triggering SCR) device has been invented to lower the trigger voltage of the SCR device. The typical design for output ESD protection circuits with LVTSCR device is shown in Fig.2a, and the device structure of the LVTSCR is shown in Fig.2b. The I-V characteristics of the LVTSCR device in the submicron CMOS technology is illustrated in Fig.2c. In Fig.2c, the trigger voltage of the LVTSCR may be decreased to about 10V. In previous designs using SCR or LVTSCR devices, the body of the SCR or LVTSCR devices is the common p-substrate 14, which is commonly grounded, as shown in Figs.1b and 2b. Therefore, they serve only as routes from the input/output (I/O) pads to VSS or VDD power lines as I/O ESD protection circuits, or from VDD to VSS as a VDD-to-VSS ESD clamp circuit.

To provide high-noise immunity in analog or RF IC, a CMOS process often supports an additional deep N-well structure to isolate the P-well from the grounded p-substrate. Because noise generated from the digital circuits is often coupled into the common P-type substrate, signals in the high-performance analog circuits or the critical DRAM memory cells are easily affected by the coupled noises from the P-type substrate. To overcome the noise issue, a CMOS process often provides an additional deep N-well structure to isolate NMOS in the memory array from the periphery circuits. However, once the noise triggers the SCR and LVTSCR in Figs.1a and 2a, the signal voltage on the I/O pad will be latched up and the actual signals will not be detected correctly.

#### SUMMARY OF THE INVENTION

A novel object of the present invention is to provide a new SCR structure having the ability to be stacked in series.

Another object of the present invention is to protect IC from ESD stress at the input, output, or power pads and free from the latch-up issue.

According to the object described above, the present invention provides a novel ESD protection component, located on a P-substrate coupled to a relatively low-voltage power source. The ESD protection component comprises a lateral silicon controlled rectifier (SCR) and a deep N-well. The SCR comprises a P-type layer (as an anode of the SCR), an N-type layer (as a cathode of the SCR) a first N-well and a first P-well. The first N-well is located between the P-type layer and the N-type layer and is contacted with the P-type layer. The first P-well is contacted with the first N-well and the N-type layer. The deep

N-well is located between the first P-well and the P-substrate, for isolating the electric connection between the P-substrate and the first P-well.

The present invention further provides an ESD protection circuit coupled between a first connection pad and a second connection pad. The ESD protection circuit comprises an ESD protection component having an anode and a cathode. The ESD protection component is located on a P-substrate coupled to a relatively low-voltage power source and comprises a lateral SCR and a deep N-well. The lateral SCR comprises: a P-type layer, as the anode of the SCR; an N-type layer, as the cathode of the SCR; a first N-well, located between the P-type layer and the N-type layer and contacted with the P-type layer; and a first P-well, contacted to the first N-well and the N-type layer. The deep N-well is located between the first P-well and the P-substrate for isolating the electric connection between the P-substrate and the first P-well. Wherein during an ESD event, the anode and the cathode are respectively connected to the first connection pad and the second connection pad.

The advantage of the present invention is that the deep N-well equivalently increases the resistor between the first p-well and the p-substrate. Moreover, after an appropriate design, the electric connection between the P-substrate and the first P-well is isolated. A plurality of the ESD components in the present invention can be connected to increase the total holding voltage, thereby preventing the latch-up event.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention can be more fully understood by reading the subsequent detailed description in conjunction with

the examples and references made to the accompanying drawings,  
wherein:

Fig. 1a is a traditional input ESD protection circuit with  
the LSCR circuit as the main ESD protection component;

5 Fig.1b is a cross-sectional diagram of the LSCR device  
structure shown in Fig.1a;

Fig.1c is the IV curve of the LSCR of Fig.1a;

Fig. 2a is the typical design of an ESD protection circuit  
with the LVTSCR device;

10 Fig.2b is a cross-sectional diagram of the LVTSCR device in  
Fig.2a;

Fig.2c is the IV curve of the LVTSCR in Fig.2b

15 Figs.3a and 3b show the cross-sectional diagrams and the  
symbols defined of the NSCR devices of the present invention;

Figs.4a and 4b show the cross-sectional diagrams and the  
symbols defined of the PSCR devices of the present invention;

Fig.5 shows another NSCR device of the present invention;

Fig.6 shows another NSCR device of the present invention;

20 Fig.7 shows the VDD-to-VSS ESD clamp circuit with the  
proposed NSCR device of the present invention;

Fig.8 is an example showing the ESD-detection circuit in  
Fig.7;

Fig.9 shows a VDD-to-VSS ESD clamp circuit with the proposed  
PSCR device of the present invention;

25 Fig.10 is an example showing the ESD-detection circuit in  
Fig.9;

Fig.11 shows the embodiment with mixed design of the  
proposed NSCR and PSCR devices in stacked configuration;

30 Figs.12 and 13 show the VDD-to-VSS ESD clamp circuit with  
the proposed NSCR equipped with diodes in stacked configuration;

Figs.14 and 15 show the VDD-to-VSS ESD clamp circuit with the proposed PSCR equipped with diodes in stacked configuration;

Fig.16 shows the proposed NSCR and PSCR devices applied to the input ESD protection circuit;

5 Fig.17 is a circuit design example showing the input ESD protection circuit in Fig.16;

Fig.18 shows the proposed NSCR and PSCR devices applied to the output ESD protection circuit;

10 Fig.19 is a circuit design example showing the input ESD protection circuit in Fig.18;

Fig.20 shows the proposed NSCR and PSCR devices applied to the input ESD protection circuit;

Fig.21 is a circuit design showing the proposed NSCR and PSCR devices for output ESD protection;

15 Fig.22 shows the application of the proposed NSCR and PSCR devices with stacked diodes in the ESD protection circuit across the separated VDD (VSS) power lines; and

Fig.23 shows another embodiment using the proposed NSCR and PSCR devices with stacked diodes in the ESD protection circuit 20 across the separated VDD (VSS) power lines.

#### **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

The embodiments described below utilize a deep N-well and a common P-substrate to implement the present invention. The 25 embodiments utilizing a deep P-well and a common N-substrate according to the present invention are familiar to those in the art after reading this specification and are not repeated here.

The first embodiment

The device structure of the proposed N-type SCR devices with the deep N-well region is shown in Fig. 3a, where a novel symbol 5 is defined in the right-hand side for the following circuit design. The N-type SCR device (hereinafter described as NSCR) has three nodes: the anode, the cathode and the gate ( $V_{GN}$ ). The PNPN structure of the NSCR is comprised of a P-well 38, an N-well 42, a P-well 40 and an N+ diffusion 46, wherein the P-well 38 and the P+ diffusion 52 are the anode of the NSCR. The P-well 40 is isolated from the common P-substrate 30 by a deep N-well 10 32 under the whole NSCR device. An NMOS is inserted into the P-well 40 of the NSCR device. The drain of the NMOS is formed by an N+ diffusion 44 across the P-N junction between the N-well 15 42 and the P-well 40. The source of the NMOS is the N+ diffusion 46, which is also the cathode of the NSCR device. The deep N-well region 32 is placed between the whole PNPN structure and the P-substrate 30, and is biased at VDD through the connection of the N-well 34. In a practical layout, the N-well 34 connected 20 to VDD usually encloses the whole NSCR device. The P-substrate 30 is connected to VSS through the P-well 36 and the p+ diffusion 54. Thereby, the body of the NSCR device is fully isolated from the p-substrate 30.

The gate of the NMOS is used as the control gate ( $V_{GN}$ ). When 25 a positive voltage is applied to this gate, the NMOS is turned on to conduct the trigger current into the p-well 40. The trigger current into the p-well 40 will fire the latch-up positive-feedback regeneration process to turn on the SCR device. The voltage difference between the anode and the cathode is kept at 30 the holding voltage (~1V). The conducting path in the SCR device

is shown by the dashed line in Fig. 3a. Because the body (p-well 40) is isolated from the P-substrate 30 by the deep N-well 32, the trigger current (from the N+ diffusion 44 of the turned-on NMOS) into the p-well 40, is not diverted. Therefore, the proposed N-type SCR provides much faster and efficient turn-on for ESD protection purposes. In the traditional LVTSCR device in Fig. 2b, the body of the LVTSCR is the common P-substrate 14. When the NMOS is turned on to generate the trigger current into the p-substrate 14 of the traditional LVTCSR device, the trigger current is diverted into the whole p-substrate. This is a main difference between the proposed NSCR with the deep N-well structure and the traditional LVTSCR device. With the isolated body, the trigger current is not diverted into the p-substrate, therefore the trigger current flows in the p-well to trigger the NSCR device earlier. This proposed NSCR device with the deep N-well structure is therefore more quickly turned on than traditional LVTSCR devices with the common p-substrate. Because the ESD events often have very fast electrical transitions in the order of several nanoseconds (ns), the ESD protection device used to bypass the ESD current must be turned on as quickly as possible to discharge the ESD current. The proposed SCR device has a faster turn-on speed, which is more suitable for ESD application.

Similar to Fig. 3a, Fig. 3b is the other embodiment of the NSCR device of the present invention, where a novel symbol is defined in the right-hand side for the following circuit design. The P-well 38 in Fig. 3a is replaced by the N-well 42 in Fig. 3b. Therefore, the P+ diffusion 52 (the anode) is formed in the N-well 42. The PNPN structure of the NSCR is composed of a P+ diffusion 52, an N-well 42, a P-well 40 and an N+ diffusion 46. The P+ diffusion 52 is isolated from the P-substrate 30 by the N-well

42, therefore, seeing the left-hand side of Fig. 3b, the N+ diffusion 50, the N-well 34 and the corresponding VDD contact can be omitted without affecting the embodiment of the present invention.

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#### The second embodiment

Based on the same concept, a P-type SCR device (herein described as PSCR) with the deep N-well structure can be built in Fig.4a, where a symbol shown in the right-hand side is used to represent this PSCR device. This P-type device has three nodes: the anode, the cathode and the control gate (VGP). The PNPN structure of the PSCR comprises P-well 38, N-well 42, P-well 40 and the N+ diffusion 46. The P-well 40 is isolated from the grounded P-substrate 30 with a deep N-well 32. There is a PMOS in the N-well 42. The source (the P+ diffusion 52) of the inserted PMOS in the PSCR structure is also as the anode of the PSCR device. The drain of the PMOS formed by the P+ diffusion 56 across the PN junction between the N-well 42 and the P-well 40. The P-well 40 is coupled to the cathode through the P+ diffusion 48. The deep N-well 32 formed between the whole PNPN structure and the P-substrate 30 is connected to VDD through the N-well 34 which in the practical layout encloses the whole PSCR component. The P-substrate 30 is connected to VSS through the P-well 36 and the P+ diffusion 54. Therefore, the body of the PSCR device is electrically floated on the grounded P-type substrate 30. When a relatively negative voltage is applied to this gate, the PMOS will be turned on to conduct the trigger current into the P-well 40. The trigger current into the P-well will fire the latch up positive-feedback regeneration process to turn on the SCR device. The current conducting path in the PSCR device is shown by the

dashed line in Fig 4a. With the isolated body in the PSCR device, the trigger current generated from the PMOS is not diverged into the common P-substrate 30, which is the main difference between this proposed PSCR with the deep N-well structure and the 5 traditional LVTSCR device. Therefore, the PSCR can be turned on more quickly for effective ESD protection.

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Similarly to Fig.4a, Fig.4b is another embodiment of the PSCR device of the present invention, where a symbol is defined at the right hand side for the following circuit design. The P-well 38 in Fig.4a is encroached and replaced by the N-well 42 in Fig.4b. Therefore, the P+ diffusion 52, as the anode, is formed inside the N-well 42. The PNPN structure of the PSCR device is comprised of P+ diffusion 52, an N-well 42, a P-well 40 and an N+ diffusion 46. The P+ diffusion 52 is isolated by the N-well 42, such that, as shown on the left side of Fig. 4b, the heavy-doped N+ diffusion 50, the N-well 34 and the corresponding VDD contact can be omitted without affecting the embodiment of the present invention.

20 The third embodiment

The modified embodiment of the NSCR device with a deep N-well is shown in Fig. 5. There are three nodes in the NSCR structure: the anode, the cathode and the control gate (VGN). The PNPN structure of the NSCR is composed of the P+ diffusion 52, the 25 N-well 42, the P-well 40 and the N+ diffusion 46. The P+ diffusion 52 is used as the anode of the NSCR device and an NMOS is inserted into the P-well 40. The drain of the NMOS is formed by the N+ diffusion 44 at the P-N junction of the P-well 40 and the N-well 42. The source of the NMOS is formed by the N+ diffusion 46, used 30 as the cathode of the NMOS device. In this modified device

structure, the P-well 40 of the NSCR device is partially connected to the common P-substrate 30. But the two deep N-well regions 3201 and 3202 are placed closer to limit the connection region of the P-well 40 and the P-substrate 30, thereby increasing the 5 equivalent resistance between them. The deep N-well 3201 is connected to N-well 60, the deep N-well 3202 is connected to N-well 42. When proper voltage is applied to the control gate VGN, the trigger current from the NMOS into the P-well 40 turns on the NSCR more quickly within the limited connection region. The current path of the NSCR device is shown by the dashed line 10 in Fig. 5.

#### The fourth embodiment

The modified device structure of the PSCR device with a deep N-well is shown in Fig. 6. In this modified PSCR structure, there are three nodes: the cathode, the anode and the control gate VGP. The PNPN structure of the PSCR device is formed by a P+ diffusion 52, an N-well 42, a P-well 40 and an N-well 60 (or an N+ diffusion 46), wherein the P+ diffusion 52 is used as the anode of the PSCR 15 device. A PMOS is inserted into the N-well 42. The drain of the PMOS is formed by the P+ diffusion 56 at the P-N junction between the P-well 40 and the N-well 42. The source of the PMOS is formed by the P+ diffusion 52, which is also the anode of the PSCR device. In this modified device structure, the P-well 40 is partially 20 connected to the common P-substrate 30. But, the two deep N-well regions 3201 and 3202 are placed closer to limit the connection region of the P-well 40 and the P-substrate 30. The deep N-well 3201 is connected to the N-well 60 and the deep N-well 25 3202 is connected to the N-well 42. With the limited connection region, the equivalent resistance between the P-well 40 and the 30

P-substrate 30 can be increased. Thereby, the trigger current from the PMOS into the P-well 40 can turn on the PSCR device more quickly.

The current path of the PSCR device is shown by the dashed line in Fig. 6. When the control gate VGP is suitably biased, the proposed PSCR device can be triggered on more quickly than the traditional LVTSCR device for more effective ESD protection applications.

10. The fifth embodiment

The VDD-to-VSS ESD clamp circuit with the proposed NSCR device is conceptually shown in Fig.7, where the control gates of the forward-stacked NSCR (NSCR\_1, NSCR\_2..NSCR\_n) are connected together and are driven by an ESD-detection circuit 70. When an ESD pulses across VDD and VSS power rails, the ESD-detection circuit 70 detects the event and sends out a high voltage to the control gate VGN to turn on the stacked N-type SCR devices NSCR\_1~NSCR\_n. The stacked NSCR devices from VDD to VSS are used to prevent the latch-up problem in CMOS IC. The forward-stacked NSCR devices NSCR\_1~NSCR\_n can be regarded as a big NSCR device with a holding voltage  $V_{hold-total}$ , equivalent to the sum of the holding voltages of all the stacked NSCR devices. Therefore, as long as the  $V_{hold-total}$  is greater than the voltage difference between VDD and VSS during normal operating conditions, the NSCR device will not be turned on to cause latch-up problems. Presuming the NSCRs are identical, the number of the NSCR devices in the forward-stacked NSCR configuration for VDD-to-VSS ESD clamp circuit without the latch-up problem can be calculated as:

$$30 \quad n \geq (VDD - VSS) / V_{hold-NSCR};$$

wherein the  $V_{hold-NSCR}$  (about 1V~2V) is the holding voltage of a single NSCR device, and n is the number of total NSCR devices in the forward-stacked SCR configuration.

A circuit design example to realize the ESD-detection circuit of Fig.7 is shown in Fig.8, where a RC delay circuit is used to distinguish the ESD event or VDD power-up event across VDD and VSS power lines. The CMOS inverter is configured as a driver. During normal operating conditions, the RC circuit initially keeps the input node of the inverter of the ESD circuit at a high-voltage level, therefore the CMOS inverter generates a low voltage output to turn off all the NMOS in the NSCR devices. In the event of an ESD, the RC circuit initially keeps the input node of the inverter of the ESD-detection circuit at a low level, and the inverter biased by the ESD energy well generates a high voltage output to the control gate VGN to simultaneously turn on the stacked NSCR devices. The ESD across the power rail is thus discharged through the turned-on stacked NSCR devices. To distinguish the ESD from normal operating conditions, the RC time constant is about 0.1~1 s.

The PSCR device can be also applied in the VDD-to-VSS ESD clamp circuit, such as that shown in Fig.9. The control gates of the forward-stacked PSCRs (PSCR\_1, PSCR\_2...PSCR\_n) are connected together and are driven by an ESD-detection circuit 74.

5 When an ESD pulses across VDD and VSS power rails, the ESD-detection circuit 74 detects the ESD event and send out a low voltage to the control gate VGP to turn on the stacked PSCRs (PSCR\_1~PSCR\_n).

A circuit design example to realize the ESD-detection circuit of Fig.9 is shown in Fig.10, where an RC delay circuit is used to distinguish an ESD or a power-up event across VDD and VSS power lines. The CMOS inverters are configured as a driver. Under normal operating conditions, the RC circuit initially keeps the input node of the inverter of the ESD-detection circuit at a high-voltage level, and the driver generates a high voltage output to turn off all the PMOS in the PSCR devices. In the event of an ESD, the RC delay circuit initially keeps the input node of the driver of the ESD-detection circuit at a low level, and, the driver biased by the ESD energy generates a low voltage output 20 to the control gate VGP to simultaneously turn on the stacked PSCR devices. The ESD across the power rail is then discharged through the turn-on stacked PSCR devices. To distinguish an ESD event from normal operating conditions, the RC time constant is about 0.1~1 s.

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#### The seventh embodiment

A more complex design by using the mixed NSCR and PSCR devices in a stacked configuration in the VDD-to-VSS ESD clamp circuit is shown in Fig.11, where the ESD-detection circuit 76 30 has two output nodes to bias VGN and VGP, separately. During

normal operation condition, the ESD-detection circuit 76 generates a high voltage output to all the control gates VGP of the PSCR devices and a low voltage output to all the control gates VGN of the NSCR devices. When an ESD occurs across VDD and VSS power lines, the ESD protection circuit generates a low voltage output to the control gates VGP of the PSCR devices to turn on the PSCR devices, and a high voltage output to the control gates VGN of the NSCR devices to turn on the NSCR devices.

10 The eighth embodiment

This proposed NSCR can also be equipped with the diodes in the stacked configuration to overcome the latch-up problem. The design example is shown in Figs.12 and 13, where a single NSCR is stacked with multiple diodes to increase the total holding voltage greater than VDD-to-VSS voltage level. This NSCR, biased by the ESD-detection circuit 70 can be inserted in any position among the diodes. For example, the NSCR biased by the ESD-detection circuit is placed at the top of the stacked configuration (in Fig.12), or at the bottom of the stacked configuration (in Fig.13). During an ESD event, the ESD-detection circuit 70 generates a high voltage output to turn on the NMOS of the NSCR devices.

25 The ninth embodiment

This proposed PSCR can be also cooperated with the diodes in the stacked configuration to overcome the latch-up problem. The design example is shown in Figs.14 and 15, where a single PSCR is stacked with the multiple diodes to increase the total holding voltage greater than VDD-to-VSS voltage level. This PSCR biased by the ESD-detection circuit 74 can be inserted in any position

among the diodes. For example, the PSCR biased by the ESD-detection circuit is placed at the top of the stacked configuration (in Fig.14), or at the bottom of the stacked configuration (in Fig.15). During an ESD event, the ESD-detection circuit 74 generates a low voltage output to turn on the PMOS of the PSCR devices.

#### The tenth embodiment

The proposed NSCR/PSCR devices can also be applied to the input or output ESD protection circuit. Fig.16 conceptually shows the design of the input ESD protection circuit with the stacked NSCR/PSCR devices. A circuit design example to realize the design of Fig.16 is shown in Fig.17, where the forward stacked PSCR devices (PSCR\_1~PSCR\_n) are configured between the input pad 84 and VDD and the forward stacked NSCR devices (NSCR\_1~NSCR\_n) are configured between the input pad 84 and VSS. The control gate VGN of the NSCR devices (NSCR\_1~NSCR\_n) is controlled by the ESD-detection circuit 82 and the control gate VGP of the PSCR devices (PSCR\_1~PSCR\_n) is controlled by the ESD-detection circuit 80. The coupled RC circuit in the ESD-detection circuit 80 or 82 detects ESD events. When a positive ESD voltage pulse occurs at the input pad 84 with VSS relatively grounded, sharp rising ESD voltage is coupled through the capacitor Cn to the control gate VGN of the stacked NSCR devices (NSCR\_1~NSCR\_n). Therefore, the stacked NSCR devices will be turned on to discharge the ESD current from the input pad 84 to VSS. On the contrary, when a negative ESD voltage pulse occurs at the input pad 84 with VDD relatively grounded, the sharply falling negative ESD voltage is coupled through the capacitor Cp to the control gate VGP of the stacked PSCR devices. Therefore, the stacked PSCR devices

will be turned on to discharge the ESD current from VDD to the input pad 84. The number n of the NSCRs or PSCRs in the stacked configuration is dependent on the maximum voltage difference between the input pad 84 and VDD or the maximum voltage difference 5 between the input pad 84 and VSS during normal operation.

The proposed NSCR or PSCR devices can also be applied to the output ESD protection circuit, as shown in Fig.18. The circuit design example with the RC coupled circuit as the ESD-detection circuit is shown in Fig.19. The output pad is driven by an output buffer 85. The forward stacked PSCR devices (PSCR\_1~PSCR\_n) are configured between the output pad 86 and VDD; the forward stacked NSCR devices (NSCR\_1~NSCR\_n) are forward connected between the output pad 86 and VSS. The gate VGN of the stacked NSCR devices is controlled by the ESD-detection circuit 82 and the gate VGP of the stacked PSCR devices is controlled by the ESD-detection circuit 80.

#### The eleventh embodiment

The modified design with SCR-diode stacked configuration 20 for the input ESD protection circuit is shown in Fig.20, and for the output ESD protection circuit is shown in Fig.21. The NSCR\_1 is stacked with a plurality of diodes Dn\_2~Dn\_k, and the PSCR\_1 is stacked with a plurality of diodes Dp\_2~Dp\_k. The stacked configuration can be formed by multiple SCR with multiple diodes 25 depending on the holding voltage, but is not limited to a single NSCR, PSCR device or diode.

#### The twelfth embodiment

For a more comprehensive ESD protection design, an ESD clamp 30 device is also added across separate power lines VDD (or VSS) to

5 avoid ESD damage located at the internal circuits. The separate power lines are configured so that the noise generated from one circuit group will not interfere with the other circuit group through the power lines. However, the separated configuration of the power lines may also induce unexpected ESD damage. The ESD protection circuit must thereby be placed between the separated power lines. The applications of the proposed NSCR and PSCR devices with stacked diodes in the ESD connection circuits between the separated VDD or VSS power lines are shown in Fig.22 and Fig.23. The two-way ESD protection circuits 90 and 92 are placed between VDDH and VDDL, and VSSH and VSSL. In Fig.22, a single PSCR (PSCR\_1) is added into a diode string (Dp\_2~Dp\_k) in a stacked configuration from VDDH to VDDL to block noise or leakage current between the two separated VDD power lines. A single NSCR (NSCR\_1) is added into a diode string (Dn\_2~Dn\_k) in a stacked configuration from VSSH to VSSL to block the noise or leakage current between these two separated VSS power lines. When a positive voltage pulse occurs at VDDH while VDDL is grounded, the ESD-detection circuit 94 sends a relatively negative voltage 10 to the PMOS in PSCR\_1 to trigger on the PSCR\_1. The diode Dp\_a is applied for ESD protection when a negative voltage pulse occurs at VDDH while VDDL is grounded. When a positive voltage pulse happens at VSSH while VSSL is grounded, the ESD-detection circuit 96 sends a relatively positive voltage to the NMOS in NSCR\_1 to 15 trigger on the NSCR\_1. The diode Dn\_a is applied for ESD protection when a negative voltage pulse occurs at VSSH while VSSL is grounded. The stacked configuration can be formed by multiple SCR with multiple diodes depending on the holding voltage, but is not limited to a single NSCR, PSCR device or diode.

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The thirteenth embodiment

The SCR-diode stacked configuration is used to form the ESD-connection circuit between the separated VDD (or VSS) power lines in shown in Fig.23. The two-way ESD protection circuits 90 and 92 are placed between VDDH and VDDL, and VSSH and VSSL. In Fig.23, the PSCR devices PSCR\_1 and PSCR\_3 are added into a diode string ( $D_p_2 \sim D_p_k$ ) in a stacked configuration from VDDH to VDDL to block the noise or leakage current between these two separated VDD power lines. The NSCR devices NSCR\_1 and NSCR\_3 are added into a diode string ( $D_n_2 \sim D_n_k$ ) in a stacked configuration from VSSH to VSSL to block noise or leakage current between the two separated VSS power lines. When a positive voltage pulse happens at VDDH while VDDL is grounded, the ESD-detection circuit 94 sends a relatively negative voltage to the PMOS to trigger on the PSCR\_1 and PSCR\_3. The diodes  $D_p_a$  are applied for ESD protection when a negative voltage pulse occurs at VDDH while VDDL is grounded. When a positive voltage pulse happens at VSSH while VSSL is grounded, the ESD-detection circuit 96 sends a relatively positive voltage to the NMOS to trigger on the NSCR\_1 and NSCR\_3. The diodes  $D_n_a$  are applied for ESD protection when a negative voltage pulse happens at VSSH while VSSL is grounded. The stacked configuration can be formed by multiple SCR with multiple diodes depend on the holding voltage of the ESD protection circuit 90 or 92. If a higher noise-isolation effect is required between VDDL and VDDH, the diode or PSCR numbers have to be increased in the ESD protection circuit 90. The same principle is applied to the ESD protection circuit 92.

Compared to conventional NSCR or PSCR devices where the P-well is directly connected to the P-substrate, the NSCR or PSCR of the present invention adapts the deep N-well under the P-well to increase the resistance between the P-well and the P-substrate, or further isolate the electric connection between the P-well and the P-substrate. From the above demonstration, the proposed NSCR or PSCR devices with the deep N-well structure are more suitable for stacked configuration in the ESD protection circuits. The ESD protection capability of the on-chip ESD protection circuits in CMOS IC's can therefore be effectively improved by the proposed NSCR or PSCR devices.

Finally, while the invention has been described by way of examples and in terms of the preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.